RDA5820

SINGLE-CHIP BROADCAST FM TRANSCEIVER

Rev.1.3–Oct.2008

1 General Description

The RDA5820 is a single-chip broadcast FM transceiver with fully integrated synthesizer, IF selectivity and MPX decoder. The chip uses the CMOS process, support multi-interface and require the least external component. The package size is 4X4mm and is completely adjustment-free. All these make it very suitable for portable devices.

The RDA5820 has a powerful low-IF digital audio processor, this make it have optimum sound quality with varying reception conditions.

The RDA5820 use RDA patented dual synthesizers, all digital transmit structure, this make it have perfectly transmition performance and agility.

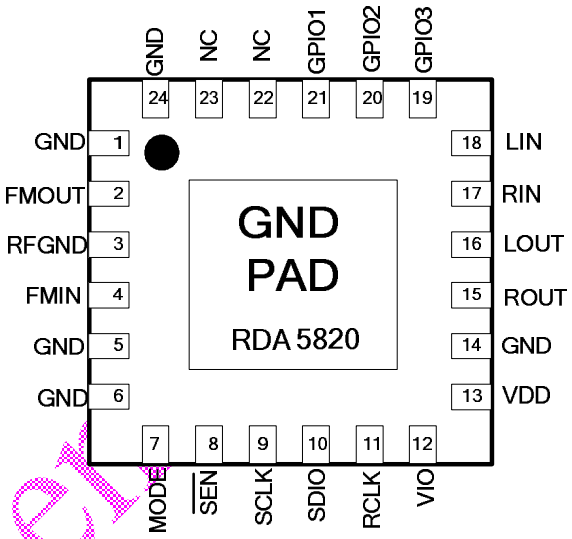


Figure 1-1. RDA5820 Top View

The RDA5820 support 65M~115M frequency band receive and transmit, integrate 4K memory, these make it can be used in simple wireless control appliance such as toy.

1.1 Features

- CMOS single-chip fully-integrated FM transceiver
- Low power consumption
  - Total current consumption lower than 20mA at 3.0V power supply
- Support worldwide and campus frequency band
  - 65 -115 MHz
- Digital low-IF tuner
  - Image-reject down-converter
  - High performance A/D converter
  - IF selectivity performed internally
- Fully integrated digital frequency synthesizer
  - Fully integrated on-chip RF and IF VCO
  - Fully integrated on-chip loop filter
- All digital transmitter
- Autonomous search tuning
- Support integrated Rx/Tx PCB antenna
- Support SNR FM searching
- Include 4K memory
- Support 32.768KHz crystal oscillator
- Digital auto gain control (AGC)
- Digital adaptive noise cancellation
  - Mono/stereo switch
  - Soft mute
  - High cut
- Programmable de-emphasis (50/75 μs)
- Receive signal strength indicator (RSSI)
- Bass boost
- Volume control
- Support I2S digital transmitter
- Support audio power amplifier (32Ω resistance

loading)
- I²S digital input / output interface
- Line-level analog output voltage
- 32.768 KHz, 12M,24M,13M,26M,19.2M,38.4MHz reference clock
- 2-wire and 3-wire serial control bus interface
- Directly support 32Ω resistance loading
- Integrated LDO regulator
  - 2.7 to 5.5 V operation voltage
- 4X4mm 24 pin QFN package

1.2 Applications

- Cellular handsets
- MP3, MP4 players
- Portable radios
- PDAs, Notebook PCs
- Wireless Toys

2 Table of Contents

3 Functional Description

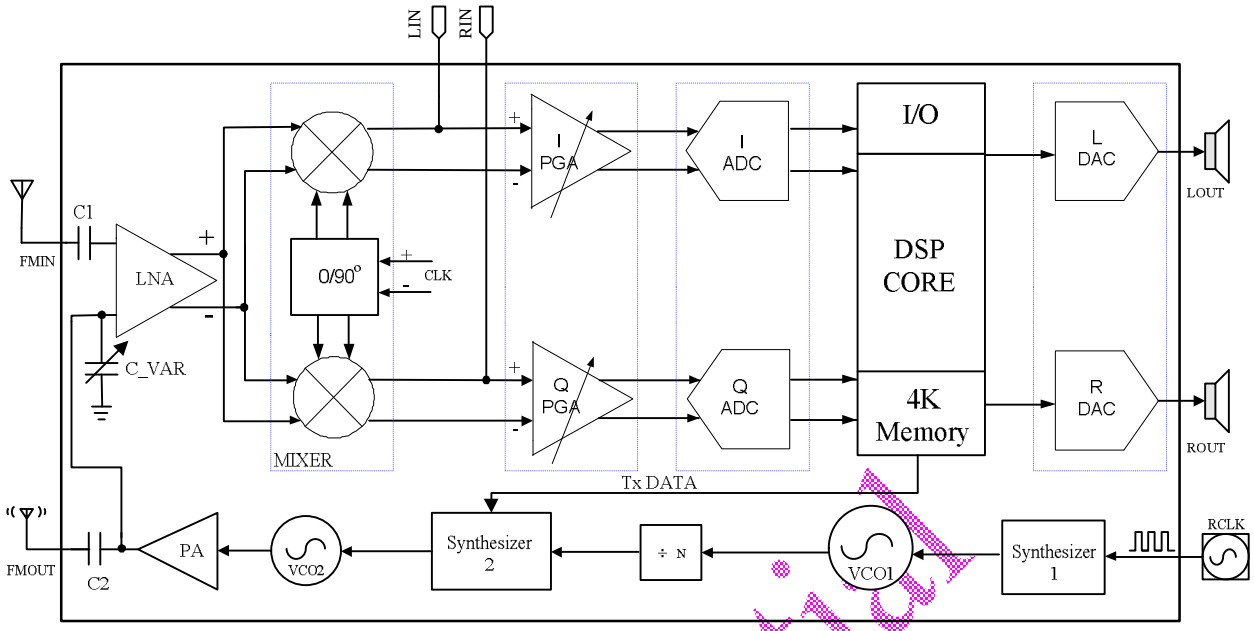


Figure 3-1. RDA5820 FM Transceiver Block Diagram

3.1 FM Transceiver Structure

The RDA5820 is a single-chip FM transceiver (Rx/Tx). Based on RDA patented dual synthesizers RF structure, it has perfectly FM receive and transmit performances, also least external components. The RDA5820 integrate 4K memory, this make it have additional advantage such as saving frequency or datas.

Except FM receive and transmit, the RDA5820 also have I2S input/output, audio amplify, integrated PCB antenna functions. All these make it very suitable for portable devices.

3.2 FM Receiver

The receiver uses a digital low-IF architecture that avoids the difficulties associated with direct conversion while delivering lower solution cost and reduces complexity, and integrates a low noise amplifier (LNA) supporting the FM broadcast band (65 to 115MHz), a quadrature image-reject mixer, a programmable gain control (PGA), a high resolution analog-to-digital converters (ADCs), an audio DSP and a high-fidelity digital-to-analog converters (DACs).

The LNA has differential input ports, one for usual FM antenna, and the other port connect with FMOUT port, which support integrated PCB antenna (small antenna). The two LNA ports can be arbitrary selected by set according registers bits (LNA_PORT_SEL[1:0]). It default input common mode voltage is GND.

The quadrature mixer down converts the LNA output differential RF signal to low-IF, it also has image-reject function.

The PGA amplifies the mixer output IF signal and then digitized with ADCs.

The DSP core finishes the channel selection, FM demodulation, stereo MPX decoder and output audio signal. The MPX decoder can autonomous switch from stereo to mono to limit the output noise.

The DACs convert digital audio signal to analog and change the volume at same time. The DACs has low-pass feature and -3dB frequency is about 30 KHz.

The PA (Power Amplifier) is power down. Its output impedance is high resistance.

If use integrated PCB antenna (small antenna), the FM signal input from FMOUT port. C_VAR is autonomous tune when setting different receive frequency.

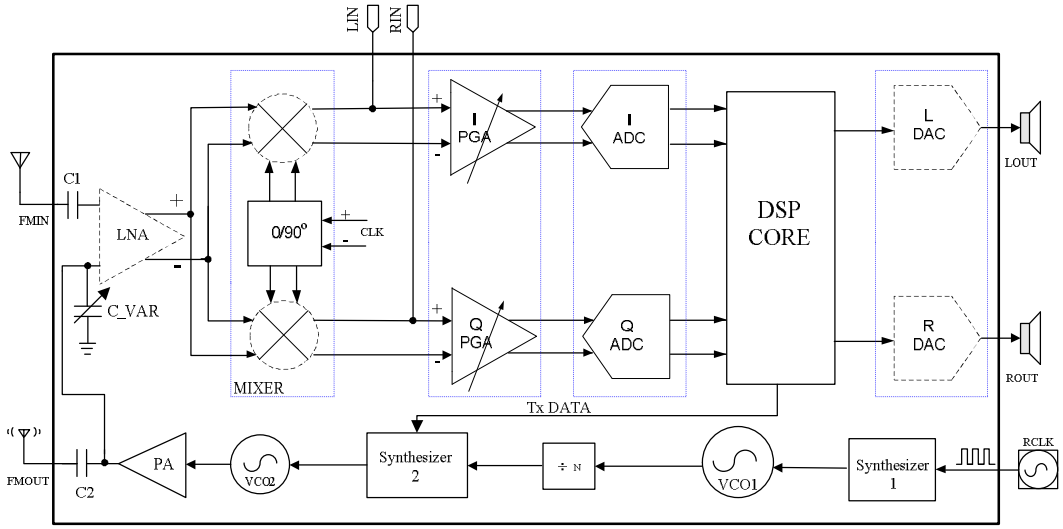


Figure 3-2. RDA5820 FM Transmit Block Diagram

3.3 FM Transmitter

The transmitter uses a digital modulate structure. Audio signals (LIN and RIN) are amplified by PGAs firstly, then converted to digital codes by ADCs. The DSP core finishes audio coding and FM modulate, pre-emphasis. The syntersizer2 transmits the digital FM data to VCO2. The PA (Power Amplifier) amplify the FM signal.

The PGA gain and PA gain are adjustable by set according registers bits (PGA_GAIN[2:0] and PA_GAIN[5:0]).

PGA_GAIN [2:0]	V-LIN(V_{PP})	**PGA_GAIN [2:0]**	V-LIN(V_{PP})
000	1.20V	100	0.075V
001	0.60V	101	0.037V
010	0.30V	110	0.018V
011	0.15V	111	0.009V

3.4 Audio Amplify

Audio signals (LIN and RIN) can also directly send to audio amplifier in DACs and driving the headphone through LOUT and ROUT ports.

3.5 I2S

The RDA5820 supports directly digital FM transmit. The digital signals can input through chip's ports GPIO1/2/3, then transmits directly through synthersizer2 and PA.

Also transmit to DAC and send out through LOUT and ROUT ports.

I2S mode support master and slave mode.

3.6 PA

The PA (Power Amplifier) work frequency band is 65~115MHz, and output power is linearly adjustable. The PA use linear structure for better frequency distortion performance.

3.7 Synthesizer1

The frequency synthesizer 1 (including synthesizer1 and VCO1) generates the local oscillator signal which divide to quadrature, then be used to downconvert the RF input to a constant low intermediate frequency (IF). The synthesizer reference clock is 32.768 KHz.

The synthesizer1 frequency is defined by bits CHAN[9:0] with the range from 65MHz to 115MHz.

The synthesizer1 also generates reference to synthesizer2 under FM TX (transmit) mode.

3.8 Synthesizer2

The frequency synthesizer 2 (including synthesizer2 and VCO2) generates clock signals for ADC under FM RX (receive) mode. The frequency synthesizer2 is also the FM transmit core. The digital signals (audio) are directly added on it.

3.9 Power Supply

The RDA5820 integrated one LDO which supplies power to the chip. The external supply voltage range is 2.7-5.5 V.

3.10 RESET and Control Interface select

The RDA5820 is RESET itself When VIO is Power up. And also support soft reset by trigger 02H BIT1 from 0 to 1. The control interface is selected by MODE Pin. The MODE Pin is low ,I2C Interface is selected. The MODE Pin is set to VIO, SPI Interface is selected.

3.11 Control Interface

The RDA5820 supports three-wire and I^2C control interface. User could select either of them to program the chip.

The three-wire interface is a standard SPI interface. It includes three pins: $\overline{SEN}$, SCLK and SDIO. Each register write is 25-bit long, including 4-bit high register address, a r/w bit, 4-bit low register address, and 16-bit data (MSB is the first bit). RDA5820 samples command byte and data at posedge of SCLK. Each register read is also 25-bit long, including 4-bit high register address, a r/w bit, 4-bit low register address, and 16-bit data (MSB is the first bit) from RDA5820. The turn around cycle between command byte from MCU and data from RDA5820 is a half cycle. RDA5820 samples command byte at posedge of SCLK, and output data also at posedge of SCLK.

The I^2C interface is compliant to I^2C Bus Specification 2.1. It includes two pins: SCLK and SDIO. A I^2C interface transfer begins with START condition, a command byte and data bytes, each byte has a followed ACK (or NACK) bit, and ends with STOP condition. The command byte includes a 7-bit chip address (0010001b) and a R/W bit. The ACK (or NACK) is always sent out by receiver. When in write transfer, data bytes is written out from MCU, and when in read transfer, data bytes is read out from RDA5820.

Details refer to *RDA5820 Programming Guide*.

3.12 I^2S Audio Data Interface

The RDA5820 supports I^2S (Inter_IC Sound Bus) audio interface. The interface is fully compliant with I^2S bus specification. When setting I2SEN bit high, RDA5820 will output SCK, WS, SD signals from GPIO3, GPIO1, GPIO2 as I^2S master and transmitter, the sample rate is 48Kbps , 44.1kbps,32kbps…… RDA5820 also support as I^2S slaver mode and transmitter, the sample rate is less than 100kbps.

3.13 GPIO Outputs

The RDA5820 has three GPIOs. The function of GPIOs could programmed with bits GPIO1[1:0], GPIO2[1:0], GPIO3[1:0] and I2SEN.

If I2SEN is set to low, GPIO pins could be programmed to output low or high or high-Z, or be programmed to output interrupt and stereo indicator with bits GPIO1[1:0], GPIO2[1:0], GPIO3[1:0]. GPIO2 could be programmed to output a low interrupt (interrupt will be generated only with interrupt enable bit STCIEN is set to high) when seek/tune process completes. GPIO3 could be programmed to output stereo indicator bit ST. Constant low, high or high-Z functionality is available regardless of the state of VA and VD supplies or the ENABLE bit.

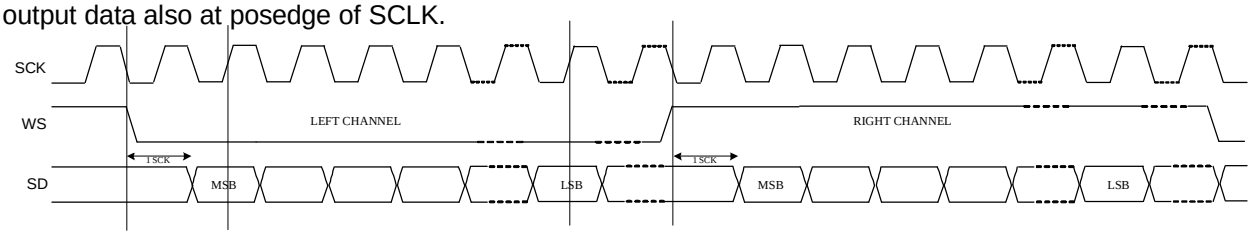


Figure 3-2. I2S Digital Audio Format

4 Electrical Characteristics

Table 4-1 DC Electrical Specification (Recommended Operation Conditions):

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
VDD	Supply Voltage	2.7	3.3	5.5	V
VIO	Interface Supply Voltage	1.5	-	3.6	V
T_{amb}	Ambient Temperature	-20	27	+70	℃
V_{IL}	CMOS Low Level Input Voltage	0		0.3*DVDD	V
V_{IH}	CMOS High Level Input Voltage	0.7*VDD		DVDD	V
V_{TH}	CMOS Threshold Voltage		0.5*VDD		V

Table 4-2 DC Electrical Specification (Absolute Maximum Ratings):

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
VIO	Interface Supply Voltage	-0.5		+4	V
T_{amb}	Ambient Temperature	-40		+90	°C
I_{IN}	Input Current (1)	-10		+10	mA
V_{IN}	Input Voltage(1)	-0.3		VIO+0.3	V
V_{lna}	LNA FM Input Level			-20	dBm

Notes:

1. For Pin: SCLK, SDIO, $\overline{SEN}$, MODE

Table 4-3 Power Consumption Specification

(VDD = 2.7 to 5.5 V, T_A = -25 to 85 ℃, unless otherwise specified)

SYMBOL	DESCRIPTION	CONDITION	TYP	UNIT
FM Receiver				
I_A	Analog Supply Current	ENABLE=1	16	mA
I_D	Digital Supply Current	ENABLE=1	3	mA
I_{VIO}	Interface Supply Current	SCLK and RCLK inactive	1	μA
I_{APD}	Analog Powerdown Current	ENABLE=0	2	μA
I_{DPD}	Digital Powerdown Current	ENABLE=0	2	μA
FM Transmitter				
I	Supply Current	PA_GAIN[5:0]=[111111];V_{RF}=3dBm	22.5	mA
I	Supply Current	PA_GAIN[5:0]=[100111];V_{RF}=0dBm	20.7	mA
I	Supply Current	PA_GAIN[5:0]=[011100]; V_{RF}=-3dBm	20	mA
I	Supply Current	PA_GAIN[5:0]=[000000]; V_{RF}=-30dBm	17	mA

5 Receiver Characteristics

Table 5-1 Receiver Characteristics

(VDD = 2.7 to 5.5 V, T_A = -25 to 85 °C, unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
General specifications						
F_{in}	FM Input Frequency	BAND=01	87		108	MHz
		BAND=10	76		91	MHz
		BAND=11	65		108	MHz
V_{rf}	Sensitivity[1,2,3]	(S+N)/N=26dB		1.5	2	μV EMF
R_{in}	LNA Input Resistance [7]			150		Ω
C_{in}	LNA Input Capacitance [7]		2	4	6	pF
$IP3_{in}$	Input IP3[4]	AGCD=1	80		-	dBμV
α_{am}	AM Suppression[1,2]	m=0.3	40	-	-	dB
S_{200}	Adjacent Channel Selectivity	±200KHz	45		-	dB
V_{AFL}; V_{AFR}	Left and Right Audio Frequency Output Voltage (Pins LOUT and ROUT)	Volume [3:0] =1111		110		mV
(S+N)/N	Maximum Signal Plus Noise to Noise Ratio[1,2,3,5]		54	60	-	dB
α_{SCS}	Stereo Channel Separation		35	-	-	dB
THD	Audio Total Harmonic Distortion[1,3,6]			0.05	0.1	%
α_{AOI}	Audio Output L/R Imbalance				0.1	dB
R_L	Audio Output Loading Resistance	Single-ended	32	-	-	Ω
Pins FMIN, FMOUT, LOUT, ROUT, LIN, RIN and NC(22,23)						
V_{com_fmin}	Pin FMIN Input Common Mode Voltage			**Float**		V
V_{com_fmout}	Pin FMOUT Input/Output Common Mode Voltage			**Float**		V
$V_{com\_lin/rin}$	Pins LIN/RIN Input Common Mode Voltage			**VDD/2**		V
$V_{com\_lout/rout}$	Audio Output Common Mode Voltage[8]		1.1	1.2	1.3	V
V_{com_nc}	Pins NC (22, 23) Common Mode Voltage		0.45	0.5	0.55	V
! The NC(22, 23) pins SHOULD BE left floating.						

Notes:

1. F_{in}=65 to 115MHz; F_{mod}=1KHz; de-emphasis=75μs; MONO=1; L=R unless noted otherwise;
2. Δf=22.5KHz;
3. B_{AF} = 300Hz to 15KHz, RBW <=10Hz;

4. $|f_2-f_1|>1MHz$, $f_0=2xf_1-f_2$, AGC disable, F_{in}=76 to 108MHz;
5. $P_{RF}=60dB_UV$;
6. Δf=75KHz.
7. Measured at V_{EMF} = 1 m V, f_{RF} = 76 to 108MHz
8. At LOUT and ROUT pins

6 Transmitter Characteristics

Table 6-1 Transmitter Characteristics

(VDD = 2.7 to 5.5 V, T_A = -25 to 85 °C, unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
General specifications						
F_{rf}	Transmit Frequency		65		108	MHz
$\triangle F$	Transmit Frequency Accuracy and Stability[2,3]			2.6		KHz
V_{RF}	Maximum Transmit Voltage	PA_GAIN=[111111]		3		dBm
V_{RF}	Minimum Transmit Voltage	PA_GAIN=[000000]		-30		dBm
	Transmit Voltage Step			3		dBm
	Transmit Voltage Stability			1		dB
	Transmit Channel Edge Power	>±100KHz Pre-emphasis off			-60	dBc
	Transmit Adjacent Channel Power	>±200KHz Pre-emphasis off			-60	dBc
	Transmit Alternate Channel Power	>±400KHz Pre-emphasis off			-60	dBc
	Transmit Emissions	In band(76 to 108MHz)			-50	dBc
C_{tune}	Output Capacitance Max			40		pF
C_{tune}	Output Capacitance Min			3		pF
	Pre-emphasis Time Constant	TX_PREMPHASIS=75 us	70	75	80	us
		TX_PREMPHASIS=50 us	45	50	55	us
	Audio SNR Mono	△f=22.5KHz,Mono Limiter off	55	60		dB
	Audio SNR Stereo	△f=22.5KHz, △fpolit=6.75KHz, Stereo Limiter off	51	56		dB
	Audio THD Mono	△f=75KHz,Mono Limiter off		0.3	0.6	%
	Audio THD Stereo	△f=68.25KHz, △fpolit=6.75KHz, Stereo Limiter off		0.3	0.6	%

	Audio Stereo Separation			40		dB
SCR	Sub Carrier Rejection Ratio			40		dB
	Power up Setting Time				100	ms
	Input Signal Level				1	V_{PK}
	Frequency Flatness	Mono,±1.5dB, $\triangle$f=75KHz, 0,50,75us pre-emphasis, limiter off	30		15K	Hz
	High-Pass Frequency Response	Mono,-3dB, $\triangle$f=75KHz, 0,50,75us pre-emphasis, limiter off	5		30	Hz
	Low-Pass Frequency Response	Mono,-3dB, $\triangle$f=75KHz, 0,50,75us pre-emphasis, limiter off	15k		16k	Hz
	Audio Imbalance	Mono	-1		1	dB
	Pilot Modulation Rate Accuracy	$\triangle$f=68.25KHz, $\triangle f_{pilot}$=6.75KHz,Stereo	-10		10	%
	Audio Modulation Rate Accuracy	$\triangle$f=68.25KHz, $\triangle f_{pilot}$=6.75KHz,Stereo	-10		10	%
	Input Resistance		25	30	35	KΩ
	Input Capacitance		0.5	0.7	1	pF

Notes:

1. F_{in}=65 to 115MHz; F_{mod}=1KHz; de-emphasis=75µs; MONO=1; L=R unless noted otherwise;
2. Guaranteed by Characterization only;
3. No measurable $\triangle f_{RF}/\triangle V_{DD}$ at $\triangle V_{DD}$ of 500mV pk-pk at 100HZ to 10KHz;

7 Serial Interface

7.1 Three-wire Interface Timing

Table 7-1 Three-wire Interface Timing Characteristics

(VDD = 2.7 to 5.5 V, T_A = -25 to 85 °C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
SCLK Cycle Time	t_{CLK}		35			ns
SCLK Rise Time	t_R				50	ns
SCLK Fall Time	t_F				50	ns
SCLK High Time	t_{HI}		10			ns
SCLK Low Time	t_{LO}		10			ns
SDIO Input, $\overline{SEN}$ to SCLK↑ Setup	t_s		10	-	-	ns
SDIO Input, to SCLK↑ Hold	t_h		10	-	-	ns
SCLK↑ to SDIO Output Valid	t_{cdv}	Read	2	-	10	ns
$\overline{SEN}$↑ to SDIO Output High Z	t_{sdz}	Read	2	-	10	ns
Digital Input Pin Capacitance					5	pF

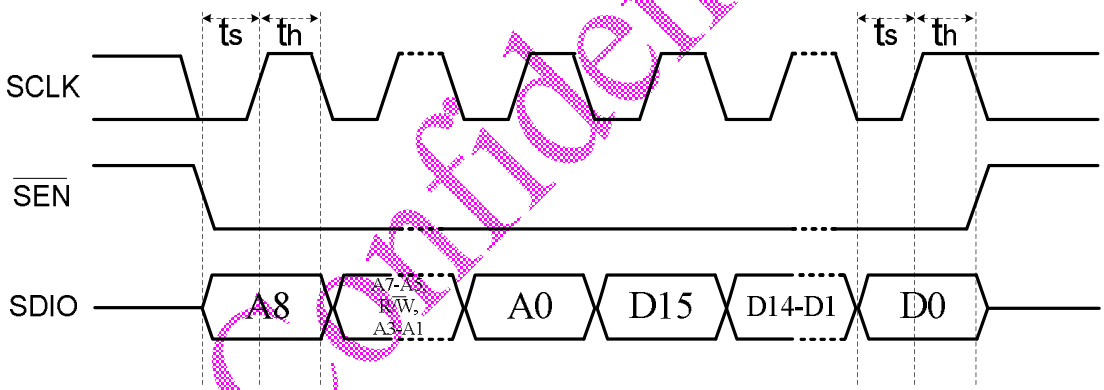


Figure 7-1. Three-wire Interface Write Timing Diagram

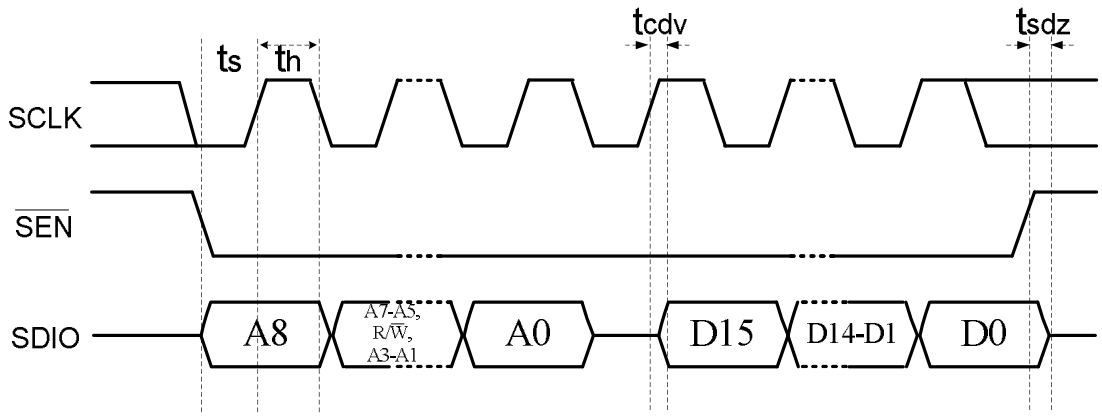


Figure 7-2. Three-wire Interface Read Timing Diagram

7.2 I²C Interface Timing

Table 7-2 I²C Interface Timing Characteristics

(VDD = 2.7 to 5.5 V, T_A = -25 to 85 °C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
SCLK Frequency	f_{scl}		0	-	400	KHz
SCLK High Time	t_{high}		0.6	-	-	µs
SCLK Low Time	t_{low}		1.3	-	-	µs
Setup Time for START Condition	$t_{su:sta}$		0.6	-	-	µs
Hold Time for START Condition	$t_{hd:sta}$		0.6	-	-	µs
Setup Time for STOP Condition	$t_{su:sto}$		0.6	-	-	µs
SDIO Input to SCLK↑ Setup	$t_{su:dat}$		100	-	-	ns
SDIO Input to SCLK↓ Hold	$t_{hd:dat}$		0	-	900	ns
STOP to START Time	t_{buf}		1.3	-	-	µs
SDIO Output Fall Time	$t_{f:out}$		$20+0.1C_b$	-	250	ns
SDIO Input, SCLK Rise/Fall Time	$t_{r:in}$ / $t_{f:in}$		$20+0.1C_b$	-	300	ns
Input Spike Suppression	t_{sp}		-	-	50	ns
SCLK, SDIO Capacitive Loading	C_b		-	-	50	pF
Digital Input Pin Capacitance					5	pF

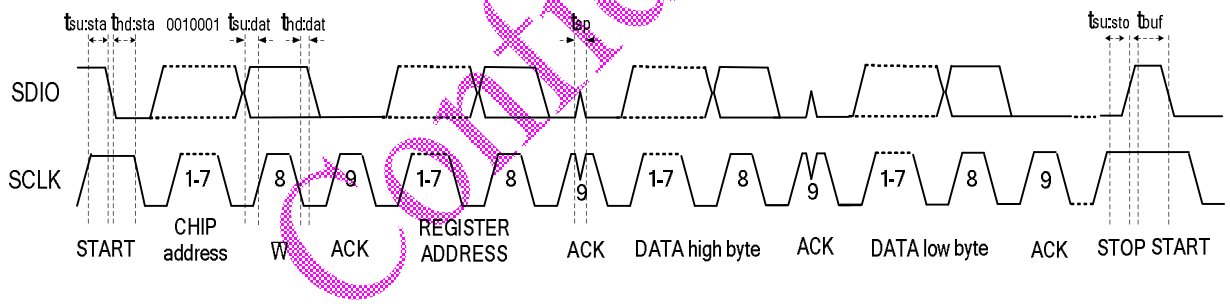


Figure 7-3. I²C Interface Write Timing Diagram

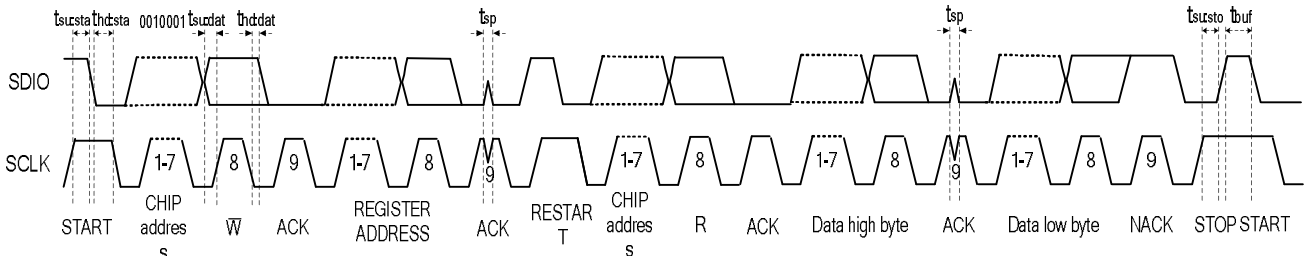


Figure 7-4. I²C Interface Read Timing Diagram

8 Register Definition

REG	BITS	NAME	FUNCTION	DEFAULT
00H	15:8	CHIPID[7:0]	Chip ID.	0x58
02H	15	DHIZ	Audio Output High-Z Disable. 0 = High impedance; 1 = Normal operation	0
	14	DMUTE	Mute Disable. 0 = Mute; 1 = Normal operation	0
	13	MONO	Mono Select. 0 = Stereo; 1 = Force mono	0
	12	BASS	Bass Boost. 0 = Disabled; 1 = Bass boost enabled	0
	9	SEEKUP	Seek Up. 0 = Seek down; 1 = Seek up	0
	8	SEEK	Seek. 0 = Disable; 1 = Enable Seek begins in the direction specified by SEEKUP and ends when a channel is found with RSSI level above SEEKTH[5:0], or the entire band has been searched. The SEEK bit is set low and the STC bit is set high when the seek operation completes.	0
	7	SKMODE	Seek Mode 0 = wrap at the upper or lower band limit and continue seeking 1 = stop seeking at the upper or lower band limit	0
	6:4	CLK_MODE[2:0]	000=32.768kHz 001=12Mhz 101=24Mhz 010=13Mhz 110=26Mhz 011=19.2Mhz 111=38.4Mhz	000
	1	SOFT_RESET	Soft reset. If 0, not reset; If 1, reset.	0
	0	ENABLE	Power Up Enable. 0 = Disabled; 1 = Enabled	0
03H	15:8	CHAN[9:0]	Channel Select. BAND = 0 Frequency = Channel Spacing (kHz) x CHAN+ 87.5 MHz BAND = 1	00_0000_0000

REG	BITS	NAME	FUNCTION	DEFAULT
			Frequency = Channel Spacing (kHz) x CHAN + 76.0 MHz CHAN is updated after a seek operation.	
	4	TUNE	Tune 0 = Disable 1 = Enable The tune operation begins when the TUNE bit is set high. The STC bit is set high when the tune operation completes. The tune bit is reset to low automatically when the tune operation completes..	0
	3:2	BAND[1:0]	Band Select. 00 = 87.0–108 MHz (US/Europe) 01 = 76–91 MHz (Japan) 10 = 76–108 MHz (Japan wide)	00
	1:0	SPACE[1:0]	Channel Spacing. 00 = 100 kHz 01 = 200 kHz 10 = 50kHz	00
04H	14	STCIEN	Seek/Tune Complete Interrupt Enable. 0 = Disable Interrupt 1 = Enable Interrupt Setting STCIEN = 1 will generate a low pulse on GPIO2 when the interrupt occurs.	0
	11	DE	De-emphasis. 0 = 75 μs; 1 = 50 μs	0
	6	I2S_ENABLED	I2S bus enable If 0, disabled; If 1, enabled.	0
	5:4	GPIO3[1:0]	General Purpose I/O 3. 00 = High impedance 01 = Mono/Stereo indicator (ST) 10 = Low 11 = High	00
	3:2	GPIO2[1:0]	General Purpose I/O 2. 00 = High impedance 01 = Interrupt (INT) 10 = Low 11 = High	00
	1:0	GPIO1[1:0]	General Purpose I/O 1. 00 = High impedance 01 = Reserved 10 = Low 11 = High	00
05H	15	INT _MODE	If 0, generate 5ms interrupt;	1

REG	BITS	NAME	FUNCTION	DEFAULT
			If 1, interrupt last until read reg0AH action occurs.	
	14:8	SEEKTH[6:0]	Seek Threshold. RSSI scale is logarithmic. 0000000 = min RSSI	000_1000
	7:6	LNA_PORT_SEL[1:0]	LNA input port selection bit: 00: no input 01: LNAN 10: LNAP 11: dual port input	10
	5:4	LNA_ICSEL_BIT[1:0]	Lna working current bit: 00=1.8mA 01=2.1mA 10=2.5mA 11=3.0mA	10
	3:0	VOLUME[3:0]	DAC Gain Control Bits (Volume). 0000=min; 1111=max Volume scale is logarithmic	1000
06H	13	I2s_ws_inv	1=invert ws when use work mode 4'b1100 0=no invert	0
	12	I2s_mode_select	If 0, master mode; If 1, slave mode.	0
	11	I2s_ws_lr	Ws relation to l/r channel. If 0, ws=0 ->r, ws=1 ->l; If 1, ws=0 ->l, ws=1 ->r.	0
	10	I2s_sclk_edge	If 0, use normal sclk internally; If 1, use inverted sclk internally.	0
	9	I2s_data_signed	If 0, I2S output unsigned 16-bit audio data. If 1, I2S output signed 16-bit audio data.	0
	3	I2s_ws_inv	If 1, invert ws output when as master.	0
	2	I2s_sclk_inv	If 1, invert sclk output when as master.	0
0AH	14	STC	Seek/Tune Complete. 0 = Not complete 1 = Complete The seek/tune complete flag is set when the seek or tune operation completes.	0
	13	SF	Seek Fail. 0 = Seek successful; 1 = Seek failure The seek fail flag is set when the seek operation fails to find a channel with an RSSI level greater than SEEKTH[5:0].	0
	10	ST	Stereo Indicator. 0 = Mono; 1 = Stereo Stereo indication is available on GPIO3 by setting GPIO1[1:0] =01.	1
	9:0	READCHAN[9:0]	Read Channel. BAND = 0 Frequency = Channel Spacing (kHz) x READCHAN[7:0]+ 87.5 MHz	00_0000_0000

REG	BITS	NAME	FUNCTION	DEFAULT
			BAND = 1 Frequency = Channel Spacing (kHz) x READCHAN[7:0]+ 76.0 MHz READCHAN[7:0] is updated after a tune or seek operation.	
0BH	15:9	RSSI[6:0]	RSSI. 000000 = min 111111 = max RSSI scale is logarithmic.	0
	8	FM TUNE	1 = the current channel is a station 0 = the current channel is not a station	0
40H	15	AUTO_SEEK	1 = auto seek mode 0 = normal	0
	3:0	CHIP_FUNC[3:0]	0000 = FM RX 0001 = FM TX 1000 = PA 1100 =I2S_DAC	0000
41H	15	MEM_CLR	1 = memory clear all 0 = normal	0
42H	10:8	Tx_PGA_Gain_bit [2:0]	001 = min 111 = max	100
	5:0	Tx_PA_Gain_bit [5:0]	00000 = min 111111 = max	100000
4BH	7:0	Chan_num[7:0]	Valid channel number in memory	000000
4CH	14:0	TX_audio_ Deviation[14:0]	Configures audio frequency deviation level. Units are in 1Hz. Default is 67.5KHz.	011_0100_1010_1010
4DH	13:0	TX_19k_Deviation[13:0]	Configures pilot tone frequency deviation level. Unit are 1Hz . Default is 6.75KHz.	00_0101_1101_1010
53H	10:0	Chan_bottom	Valid when band user defined mode, unit kHz	d650 (65Mhz)
54H	10:0	Chan_top	Valid when band user defined mode, unit kHz	d76 (76Mhz)

8 Pins Description

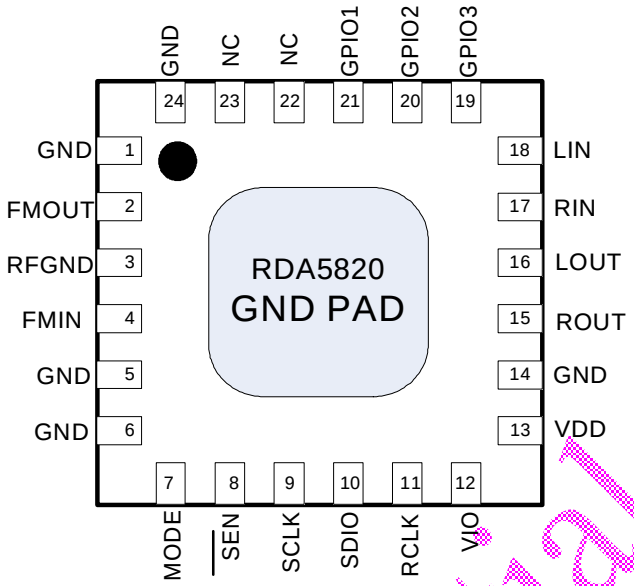
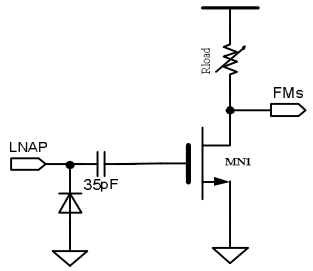
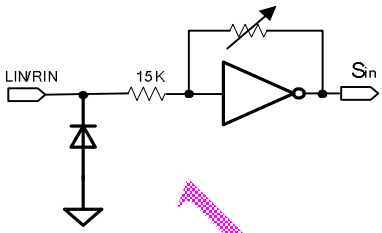
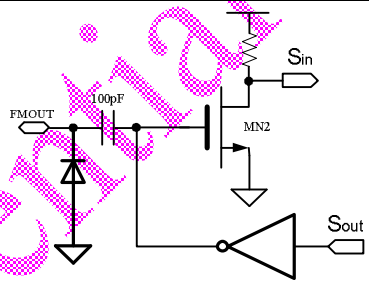
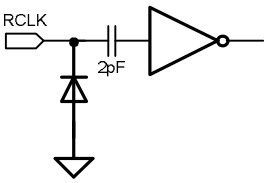
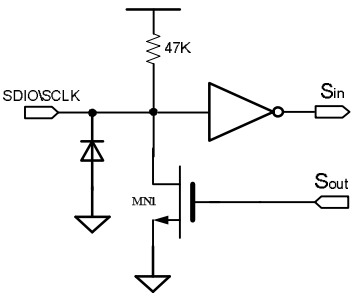
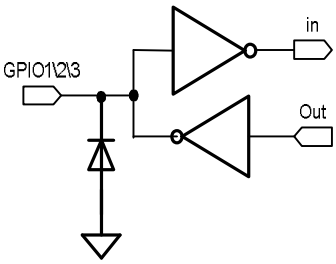


Figure 8-1. RDA5820 Top View

Table 8-1 RDA5820 Pins Description

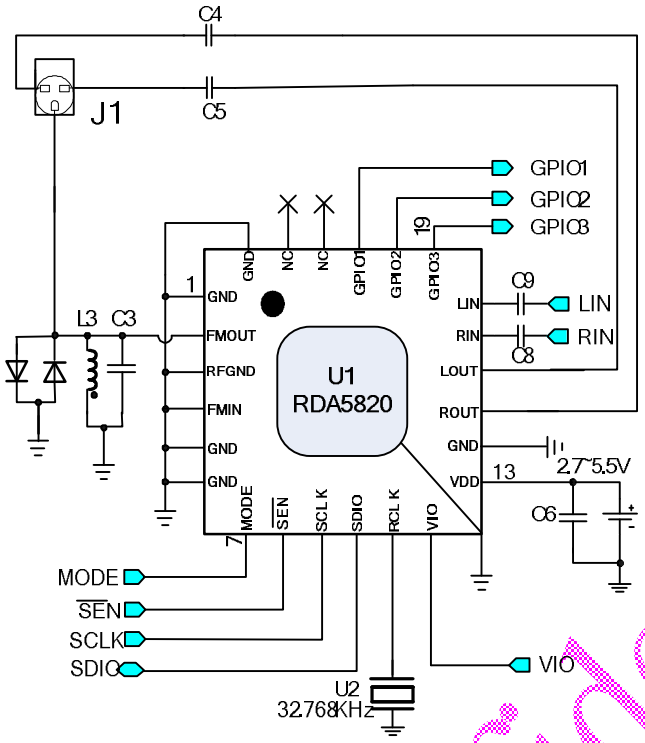
SYMBOL	PIN	DESCRIPTION
GND	1,5,6,14,24	Ground. Connect to ground plane on PCB
FMIN	4	LNA input port.
FMOUT	2	PA output port and PCB small antenna input port.
RFGND	3	LNA ground. Connect to ground plane on PCB
MODE	7	Control Interface select The MODE Pin is low ,I2C Interface is select. The MODE Pin is set to VIO, SPI Interface is select.
$\overline{SEN}$	8	Latch enable (active low) input for serial control bus
SCLK	9	Clock input for serial control bus
SDIO	10	Data input/output for serial control bus
RCLK	11	32.768KHz crystal oscillator and reference clock input
VIO	12	Power supply for I/O
VDD	13	Power supply for analog and DSP section
ROUT,LOUT	15,16	Right/Left audio output
RIN,LIN	17,18	Right/Left audio input
GPIO1,GPIO2,GPIO3	19,20,21	General purpose input/output
NC	22,23	No Connect

Table 8-2 Internal Pin Configuration

SYMBOL	PIN	DESCRIPTION
FMIN	4	
RIN/LIN	17/18	
FMOUT	2	
RCLK	11	
SCLK/SDIO	9/10	
GPIO1/GPIO2/GPIO3	19/20/21	

9 Application Diagram

9.1 Universal FM RX/TX Application Schematic:



Notes:

1. J1: Common 32Ω Resistance Headphone;
2. U1: RDA5820 Chip;
3. FM Choke (L3 and C3) for Audio Common;
4. VDD: Analog and Digital Power Supply (2.7~5.5V);
5. C8/C9: Audio Input Couple Capacitance;
6. Pins NC(22, 23), Should be Leaved Floating;
7. Set MODE to select control interface(GND—I2C,VIO—SPI);
8. Place C6 Close to VDD pin.

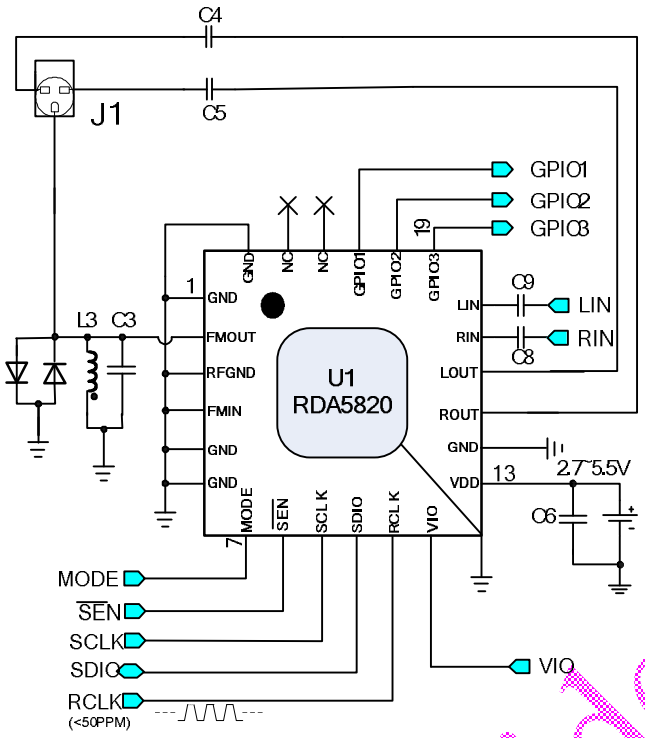
Figure 9-1. RDA5820 FM Transceiver Application Diagram

9.1.1 Bill of Materials:

COMPONENT	VALUE	DESCRIPTION	SUPPLIER
U1	RDA5820	Broadcast FM Transceiver	RDA
U2	DCXO	Crystal oscillator 32.768KHz	<=50PPM
J1		Common 32Ω Resistance Headphone	
C8/C9	0.22uF	Audio Couple Capacitors	Murata
L3/C3	100nH/24pF	LC Chock for LNA Input	Murata
C4,C5	125μF	Audio AC Couple Capacitors	Murata
C6	24nF	Power Supply Bypass Capacitor	Murata

! C8/C9 Can be Bypassed When LIN/RIN Common Mode Voltage are 1.35~1.65V

9.2 Universal FM RX/TX Application Schematic:



Notes:

1. J1: Common 32Ω Resistance Headphone;
2. U1: RDA5820 Chip;
3. FM Choke (L3 and C3) for Audio Common;
4. VDD: Analog and Digital Power Supply (2.7~5.5V);
5. C8/C9: Audio Input Couple Capacitance;
6. Pins NC(22, 23), Should be Leaved Floating;
7. Set MODE to select control interface(GND—I2C,VIO—SPI);
8. Place C6 Close to VDD pin.

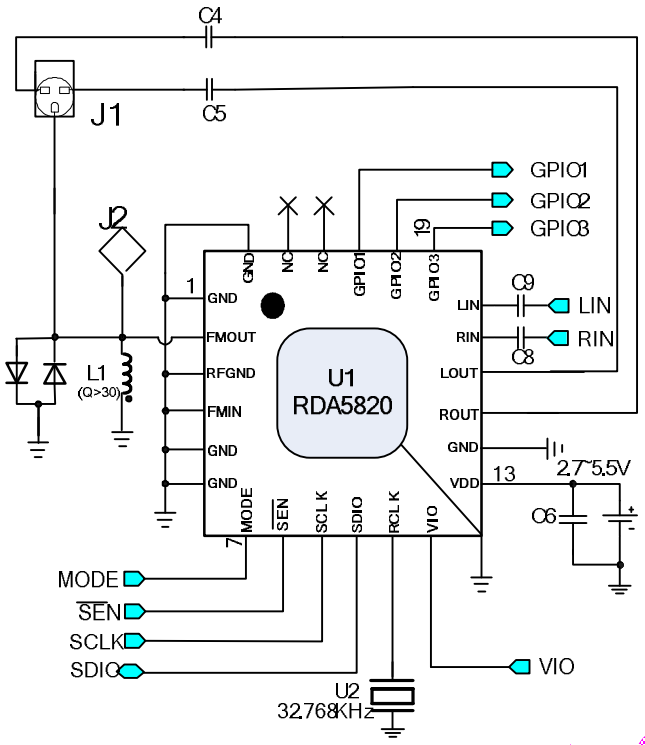
Figure 9-2. RDA5820 FM Transceiver External RCLK Application Diagram

9.2.1 Bill of Materials:

COMPONENT	VALUE	DESCRIPTION	SUPPLIER
U1	RDA5820	Broadcast FM Transceiver	RDA
J1		Common 32Ω Resistance Headphone	
C8/C9	0.22uF	Audio Couple Capacitors	Murata
L3/C3	100nH/24pF	LC Chock for LNA Input	Murata
C4,C5	125μF	Audio AC Couple Capacitors	Murata
C6	24nF	Power Supply Bypass Capacitor	Murata

! C8/C9 Can be Bypassed When LIN/RIN Common Mode Voltage are 1.35~1.65V

9.3 Universal FM RX/TX Application Schematic:



Notes:

1. J1: Common 32Ω Resistance Headphone;
2. U1: RDA5820 Chip;
3. L1: High Q Inductor for FM Tx or Integrated PCB Antenna Rx;
4. VDD: Analog and Digital Power Supply (2.7~5.5V);
5. C8/C9: Audio Input Couple Capacitance;
6. Pins NC(22, 23), Should be Leaved Floating;
7. Set MODE to select control interface(GND—I2C,VIO—SPI);
8. Place C6 Close to VDD pin.

Figure 9-3 RDA5820 FM Transceiver Application Diagram（Small PCB antenna Application）

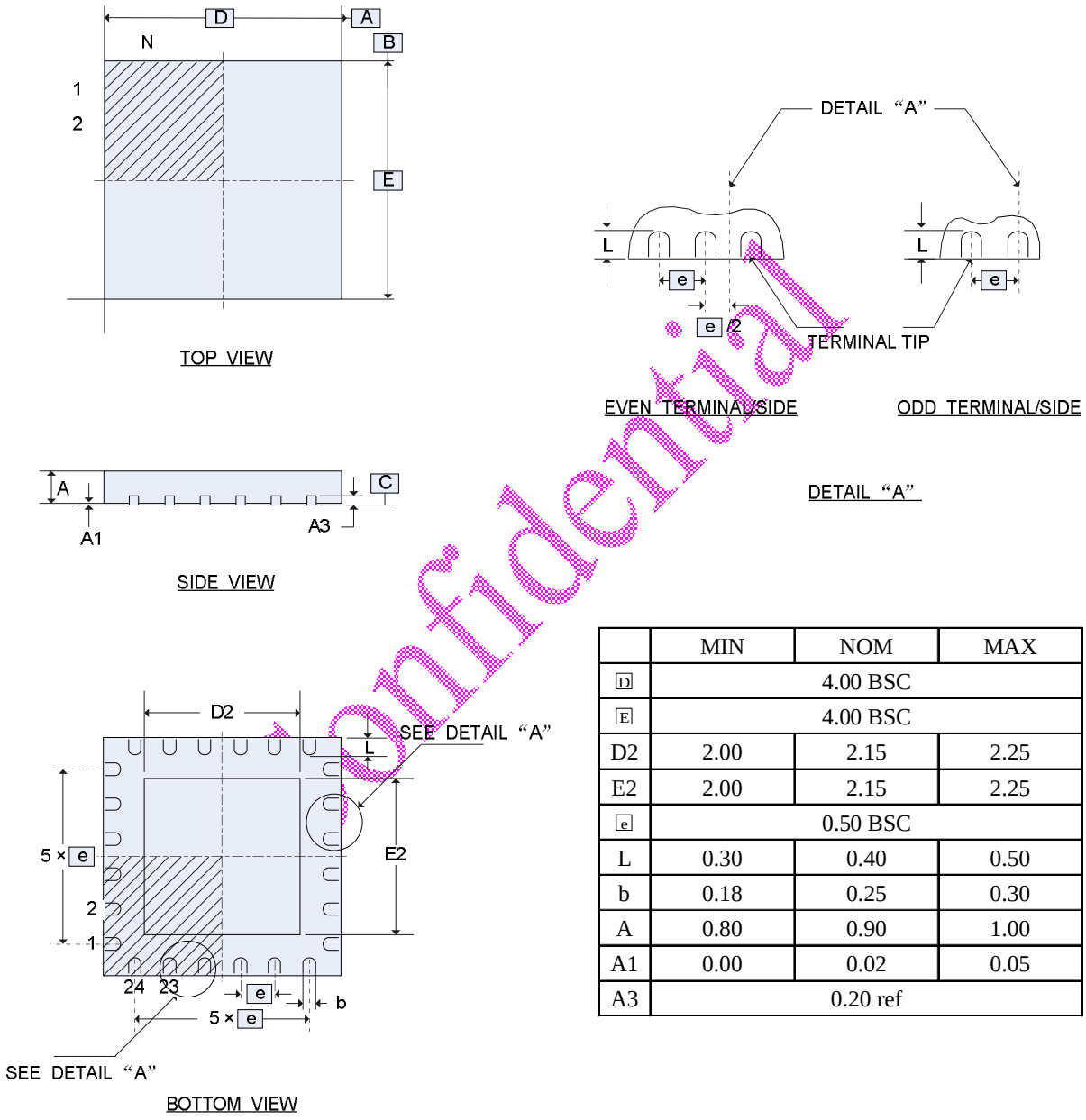
9.3.1 Bill of Materials:

COMPONENT	VALUE	DESCRIPTION	SUPPLIER
U1	RDA5820	Broadcast FM Transceiver	RDA
U2	DCXO	Crystal oscillator 32.768KHz	<=50PPM
J1		Common 32Ω Resistance Headphone	
J2		Integrated PCB antenna (small antenna)	
C8/C9	0.22uF	Audio Couple Capacitors	Murata
L1	85n~150nH	Inductor, Qmin=30	Murata
C4,C5	125μF	Audio AC Couple Capacitors	Murata
C6	24nF	Power Supply Bypass Capacitor	Murata

! C8/C9 Can be Bypassed When LIN/RIN Common Mode Voltage are 1.35~1.65V

10 Package Physical Dimension

Figure 10-1 illustrates the package details for the RDA5820. The package is lead-free and RoHS-compliant.



	MIN	NOM	MAX
D		4.00 BSC	
E		4.00 BSC	
D2	2.00	2.15	2.25
E2	2.00	2.15	2.25
e		0.50 BSC	
L	0.30	0.40	0.50
b	0.18	0.25	0.30
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3		0.20 ref	

Figure 10-2. 24-Pin 4x4 Quad Flat No-Lead (QFN)

11 PCB Land Pattern

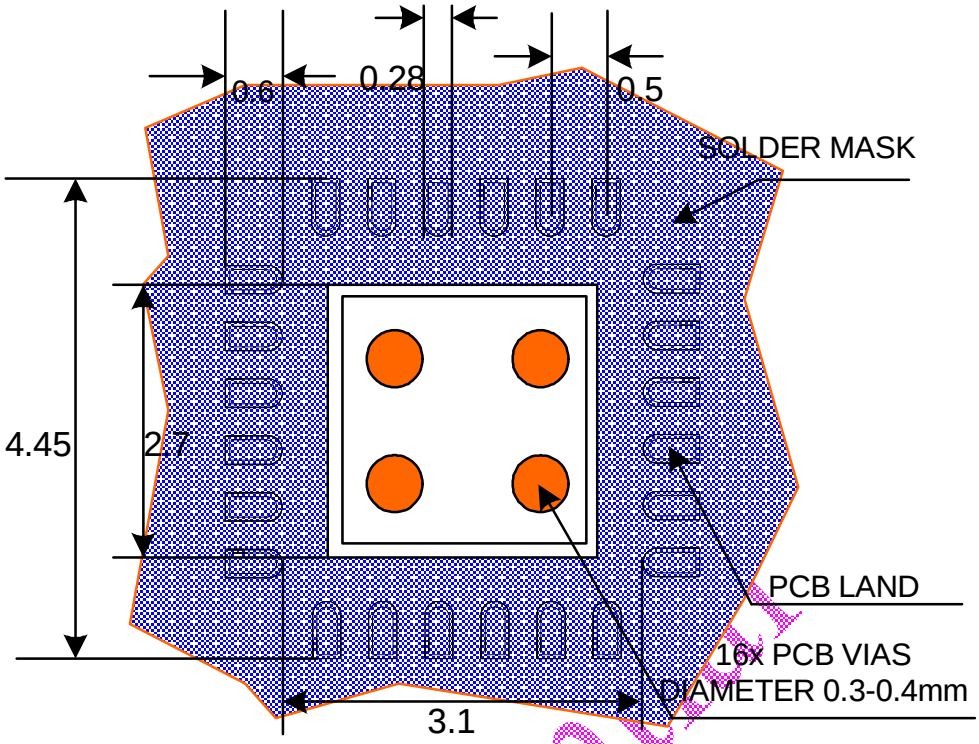


Figure 11-1. PCB Land Pattern for 24-Pin QFN

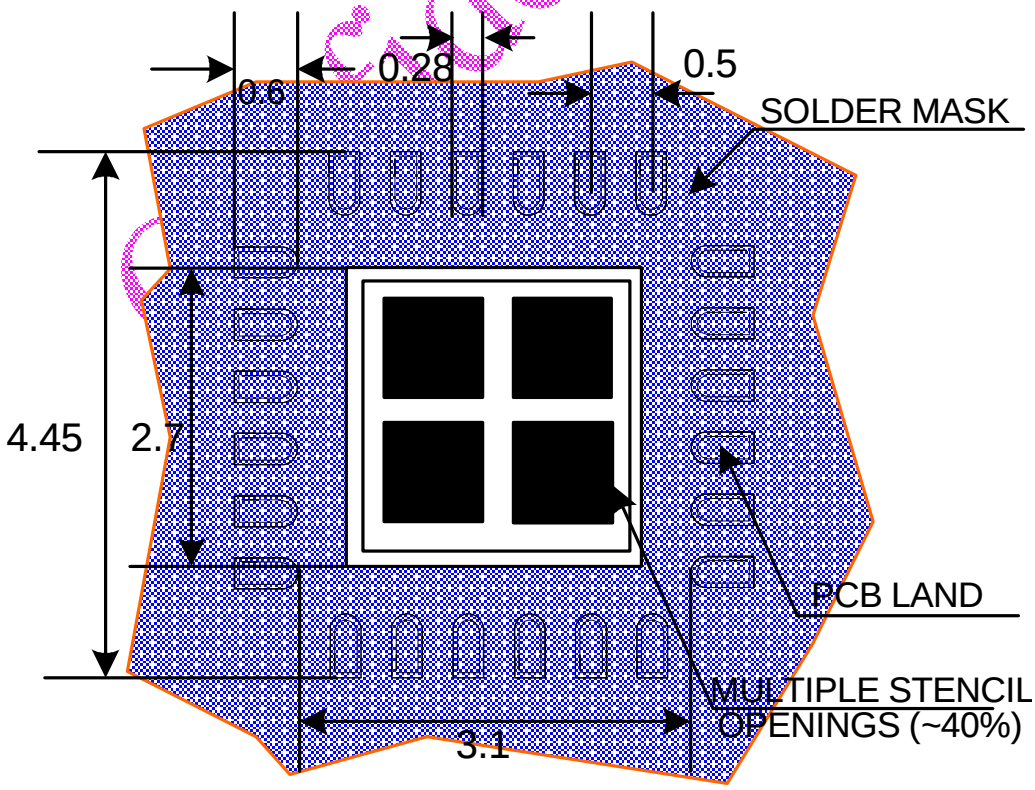


Figure 11-2. PCB Solder Paste Stencil Openings

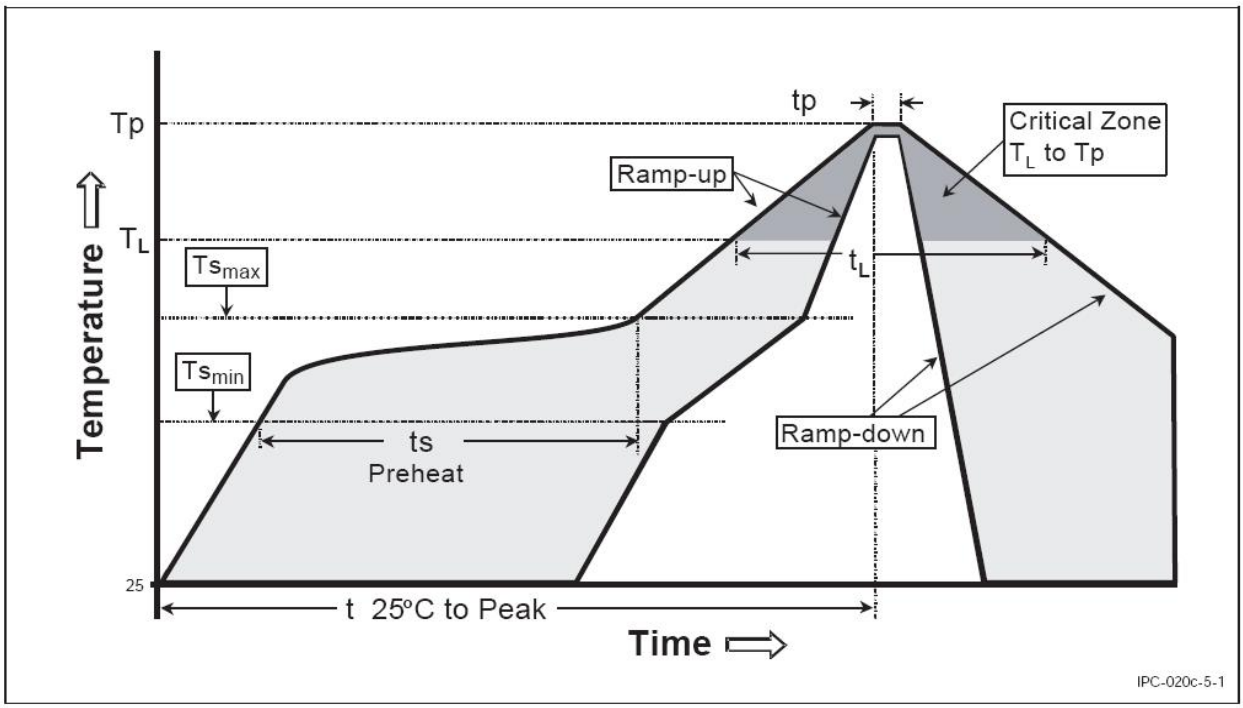


Figure 17.Classification Reflow Profile

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average Ramp-Up Rate (T_{Smax} to T_p)	3 °C/second max.	3 °C/second max.
Preheat -Temperature Min (T_{smin}) -Temperature Max (T_{smax}) -Time (t_{smin} to t_{smax})	 100 °C 100 °C 60-120 seconds	 150 °C 200 °C 60-180 seconds
Time maintained above: -Temperature (T_L) -Time (t_L)	 183 °C 60-150seconds	 217°C 60-150 seconds
Peak /Classification Temperature(T_p)	See Table-II	See Table-III
Time within 5 °C of actual Peak Temperature (t_p)	10-30 seconds	20-40 seconds
Ramp-Down Rate	6 °C/second max.	6 °C/seconds max.
Time 25 °C to Peak Temperature	6 minutes max.	8 minutes max.

Table-I Classification Reflow Profiles

Package Thickness	Volume mm^3 <350	Volume mm^3 ⩾350
＜2.5mm	240 + 0/-5 °C	225 + 0/-5 °C
⩾2.5mm	225 + 0/-5 °C	225 + 0/-5 °C

Table – II SnPb Eutectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm^3 ＜350	Volume mm^3 350-2000	Volume mm^3 ＞2000
＜1.6mm	260 + 0 °C *	260 + 0 °C *	260 + 0 °C *
1.6mm – 2.5mm	260 + 0 °C *	250 + 0 °C *	245 + 0 °C *
⩾2.5mm	250 + 0 °C *	245 + 0 °C *	245 + 0 °C *
*Tolerance : The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature(this mean Peak reflow temperature + 0 °C. For example 260+ 0 °C) at the rated MSL Level.			

Table – III Pb-free Process – Package Classification Reflow Temperatures

Note 1: All temperature refer topside of the package. Measured on the package body surface.

Note 2: The profiling tolerance is + 0 °C, - X °C (based on machine variation capability)whatever

is required to control the profile process but at no time will it exceed - 5 °C. The producer assures process compatibility at the peak reflow profile temperatures defined in Table –III.

Note 3: Package volume excludes external terminals(balls, bumps, lands, leads) and/or non integral heat sinks.

Note 4: The maximum component temperature reached during reflow depends on package the thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD package may sill exist.

Note 5: Components intended for use in a “lead-free” assembly process **shall** be evaluated using the “lead free” classification temperatures and profiles defined in Table-I II III whether or not lead free.

RoHS Compliant

The product does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB) or polybrominated diphenyl ethers (PBDE), and are therefore considered RoHS compliant.

ESD Sensitivity

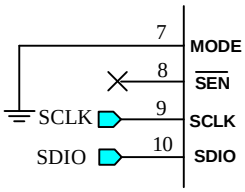
Gallium Arsenide integrated circuits are ESD sensitive and can be damaged by static electricity. Proper ESD techniques should be used when handling these devices.

12 Change List

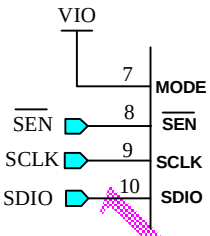
REV	DATE	AUTHER	CHANGE DESCRIPTION
V1.0	2008-09-01	ChunZhao,YananLiu,XiaoqiYou	Original Draft.

13 Notes：

1: 通过硬件电路设置芯片工作总线控制模式，详细电路如下图：



附图：I2C 总线电路接口电路



SPI 总线电路接口电路

14 Contact Information

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